



microSD 3.0 Memory Card Specification

Version 1.6

Contents

A.	General Description	2
B.	Features.....	3
C.	Comparison of SD Card.....	4
D.	Pin Assignment.....	5
E.	Power Consumption.....	7
F.	Environmental Conditions	7
G.	Electrical Specifications	7
H.	DC Characteristic.....	8
	H1. Bus Operating Conditions for 3.3V Signaling	8
	H2. Bus signal line load	9
	H3. Power Up Time	10
I.	AC Characteristic.....	11
	I1. Micro SD Interface timing (Default)	12
	I2. Micro SD Interface timing (High-speed Mode)	13
	I3. SD Interface timing (SDR12, SDR25, SDR50 and SDR104 Modes)	14
	I4. SD Interface timing (DDR50 Modes).....	16
J.	Dimension.....	18
K.	Ordering information	19

A. General Description

The Secure Digital (SD) card version 3.0 is fully compliant to the specification released by SD Card Association. The Command List supports [Part 1 Physical Layer Specification Ver3.01 Final] definitions. Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver3.0 Final] Specifications.

The SD 3.0 card is based on 9-pin interface, designed to operate at a maximum operating frequency of 208MHz. It can alternate communication protocol between the SD mode and SPI mode. It performs data error detection and correction with very low power consumption. The Card capacity could be more than 64GB and up to 2TB with ex-FAT which is called SDXC (Extended Capacity SD Memory Card).

Secure Digital 3.0 card is one of the most popular cards today based on its high performance, good reliability and wide compatibility.

B. Features

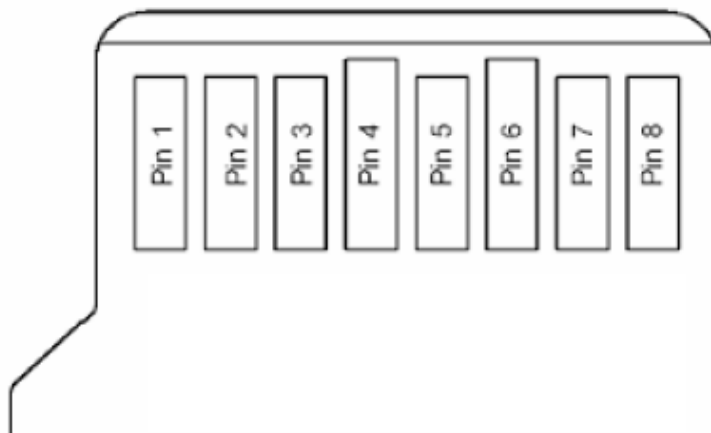
- Support SD system specification version 3.0
 - Card Capacity of Non-secure Area, Secure Area Supports [Part 3 Security Specification Ver3.0 Final] Specifications
 - Capacity of SD3.0 Memory
 - SDSC: Up to and including 2 GB
 - SDHC: More than 2GB and up to and including 32GB
 - SDXC: More than 32GB and up to and including 2TB
 - Support SD SPI mode
 - Designed for read-only and read/write cards.
 - Bus Speed Mode (using 4 parallel data lines)
 - Default Speed mode: 3.3V signaling, Frequency up to 25 MHz, up to 12.5 MB/sec
 - High Speed mode: 3.3V signaling, Frequency up to 50 MHz, up to 25 MB/sec
 - SDR12 - SDR up to 25MHz 1.8V signaling
 - SDR25 - SDR up to 50MHz 1.8V signaling
 - SDR50: 1.8V signaling, Frequency up to 100 MHz, up to 50MB/sec
 - SDR104: 1.8V signaling, Frequency up to 208MHz, up to 104MB/sec
 - DDR50: 1.8V signaling, Frequency up to 50 MHz, sampled on both clock edges, up to 50MB/sec
- Note: Timing in 1.8V signaling is different from that of 3.3V signaling.
- The Command List supports [Part 1 Physical Layer Specification Ver3.1 Final] definitions
 - Copyrights Protection Mechanism - Complies with highest security of CPRM standard
 - CPRM (Content Protection for Recordable Media) of SD Card supported.
 - Card removal during read operation will never harm the content
 - Password Protection of cards (option)
 - Write Protect feature using mechanical switch

- Built-in write protection features (permanent and temporary)
- +4KV/-4KV ESD protection in contact pads.
- Dimension : 15mm(L) x 11mm(W) x 1mm(H)
- Operating voltage range : 2.7-3.6 V
- Supported two types of wear-leveling: Dynamic and Static Wear-Leveling.

C. Comparison of SD Card

	SD3.0 Standard (Backward compatible to 2.0 host)	SD3.0 SDHC (Backward compatible to 2.0 host)	SD3.0 SDXC
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support	Support
CMD8 (SEND_IF_COND)	Support	Support	Support
CMD16 (SET_BLOCKLEN)	Support	Support (Only CMD42)	Support (Only CMD42)
Partial Read	Support	Not Support	Not Support
Lock/Unlock Function	Mandatory	Mandatory	Mandatory
Write Protect Groups	Optional	Not Support	Not Support
Supply Voltage 2.0v – 2.7v (for initialization)	Not Support	Not Support	Not Support
Total Bus Capacitance for each signal line	40pF	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

D. Pin Assignment



Micro SD memory Card Pin Assignment

pin	SD Mode			SPI Mode		
	Name	Type ¹	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line[bit2]	RSV		
2	CD/DAT3 ²	I/O/PP ³	Card Detect/ Data Line[bit3]	CS	I ³	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	V _{DD}	S	Supply voltage	V _{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V _{SS}	S	Supply voltage ground	V _{SS}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line[bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[bit1]	RSV		

(1) S: power supply, I:input; O:output using push-pull drivers; PP:I/O using push-pull drivers.

(2) The extended DAT lines(DAT1-DAT3)are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to Multi-Media Cards.

(3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT(ACMD42) command.

Name	Width	Description
CID	128bit	Card identification number; card individual number for identification. Mandatory
RCA1	16bit	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization. Mandatory
DSR	16bit	Driver Stage Register; to configure the card's output drivers. Optional
CSD	128bit	Card Specific Data; information about the card operation conditions. Mandatory
SCR	64bit	SD Configuration Register; information about the SD Memory Card's Special Features capabilities Mandatory
OCR	32bit	Operation conditions register. Mandatory.
SSR	512bit	SD Status; information about the card proprietary features Mandatory
OCR	32bit	Card Status; information about the card status Mandatory

(1) RCA register is not used (available) in SPI mode

E. Power Consumption

Table list as below is the power consumption of SD card with different type of flash memory. (PS8035 + Flash Memory)

Flash mode	Max Power up Current (uA)	Max Stand by Current (uA)	Max Read Current (mA)	Max Write Current (mA)
Single ⁽¹⁾ flash(1x8bit)	150	150	100@ 3.6V	100@ 3.6V
SDR/DDR	250	250	200@3.6V	200@3.6V

(1)Data transfer mode is single channel.

F. Environmental Conditions

- **Temperature:** -25°C to 85°C in storage/ Operating: 0°C to 70°C “C” Temp & -40C to 85C “I” Temp.
- **Humidity:** RH=93% under 25°C in operating/ RH=93% under 40°C in non-operating.
- **Drop Test:** 1.5m free fall.
- **Torque Test:** 0.15N-m or +/-2.5deg.

G. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	V _{DD} -V _{SS}	DC Power Supply	-0.3	+3.3	V
2	V _{IN}	Input Voltage	V _{SS} -0.3	V _{DD} +0.3	V
3	T _a	Operating Temperature	0	+70	V
4	T _{st}	Storage Temperature	-25	+85	V

Parameter	Symbol	Min	MAX	Unit
Operating Temperature	T _a	0	+70	V
V _{DD} Voltage	V _{DD}	2.7	3.6	V

H. DC Characteristic

H1. Bus Operating Conditions for 3.3V Signaling

- Threshold level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V _{DD}	2.7	3.6	V	
Output High Voltage	VOH	0.75*VDD		V	IOH=-2mA VDD Min
Output Low Voltage	VOL		0.125*VDD	V	IOL=2mA VDD Min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	VSS-0.3	0.25*VDD	V	
Power Up Time			250	ms	From 0V to V _{DD} min

- Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max.	Unit	Remarks
Peak voltage on all lines		-0.3	V _{DD} +0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

- Threshold Level for 1.8V Signaling

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V _{DD}	2.7	3.6	V	
Regulator Voltage	V _{DDIO}	1.7	1.95	V	Generated by V _{DD}
Output High Voltage	VOH	1.4	-	V	IOH=-2mA
Output Low Voltage	VOL	-	0.45	V	IOL=2mA
Input High Voltage	VIH	1.27	2.00	V	
Input Low Voltage	VIL	V _{SS} -0.3	0.58	V	

- Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min	Max.	Unit	Remarks
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

H2. Bus signal line load

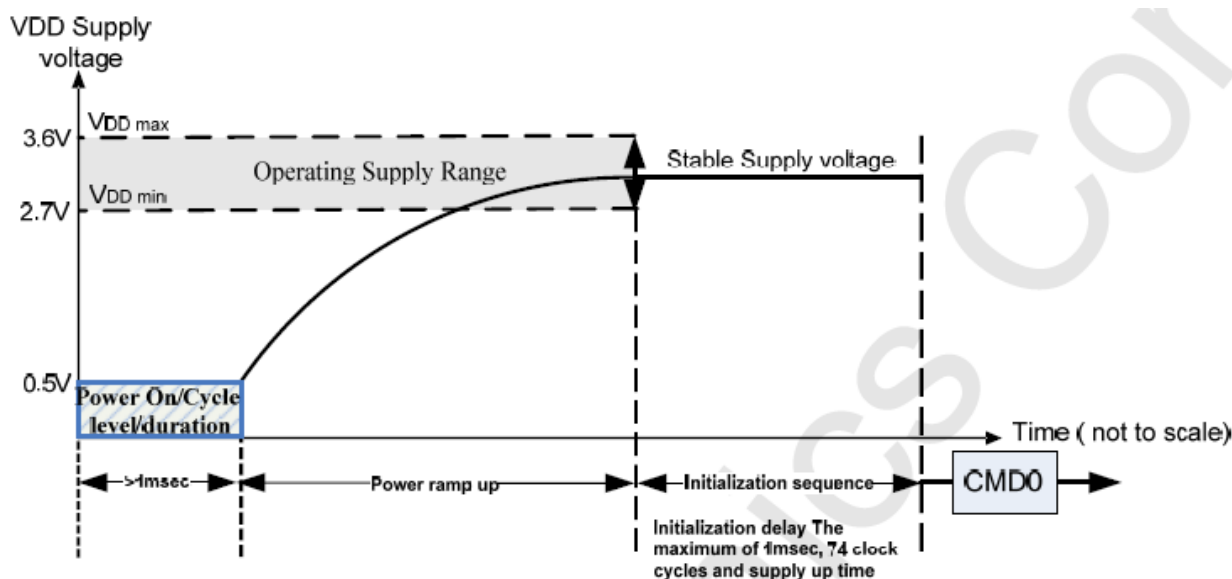
Bus Operating Conditions - Signal Line's Load

Total bus capacitance = $C_{HOST} + C_{BUS} + N \times C_{CARD}$

Parameter	symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	k Ω	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card $C_{HOST}+C_{BUS}$ shall not exceed 30 pF
Card Capacitance for each signal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	k Ω	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

H3. Power Up Time

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

- (1) Voltage level shall be below 0.5V
- (2) Duration shall be at least 1ms.

Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD(min.) and VDD(max.) and host can supply SDCLK.

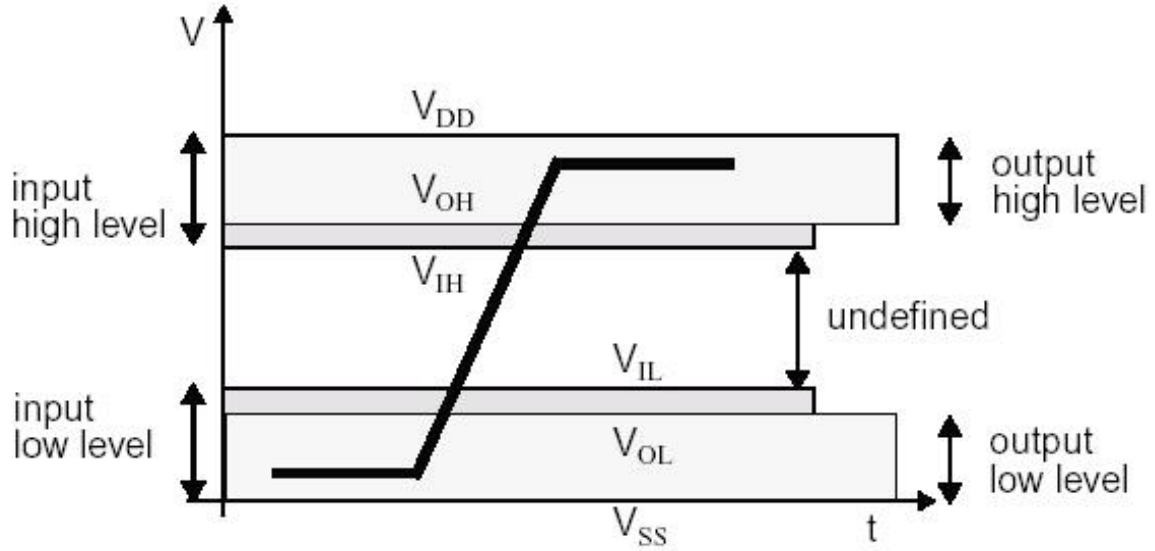
Followings are recommendation of Power ramp up:

- (1) Voltage of power ramp up should be monotonic as much as possible.
- (2) The minimum ramp up time should be 0.1ms.
- (3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.
- (4) Host shall wait until VDD is stable.
- (5) After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

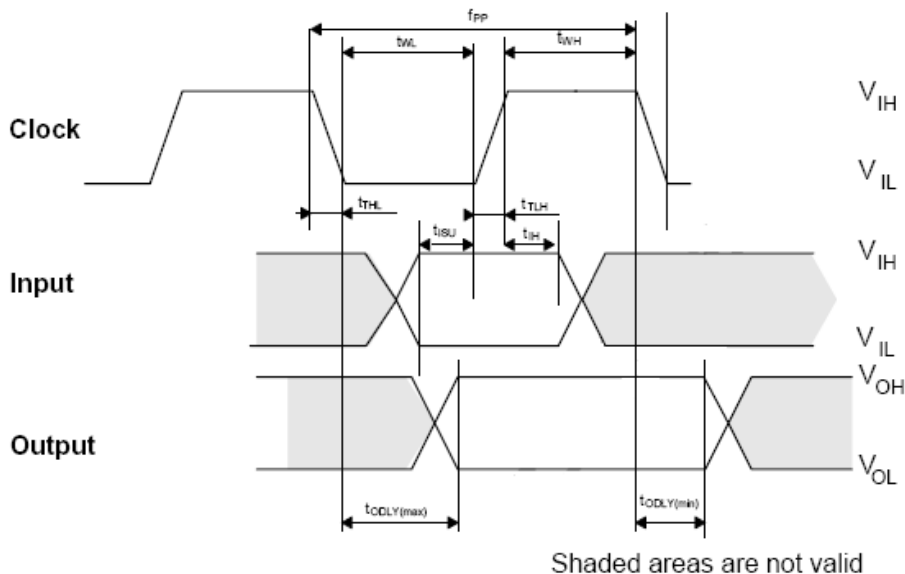
Power Down and Power Cycle

- When the host shuts down the power, the card V_{DD} shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.
- If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State*. To create a power cycle the host shall follow the power down description before power up the card (i.e. the card V_{DD} shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

I. AC Characteristic



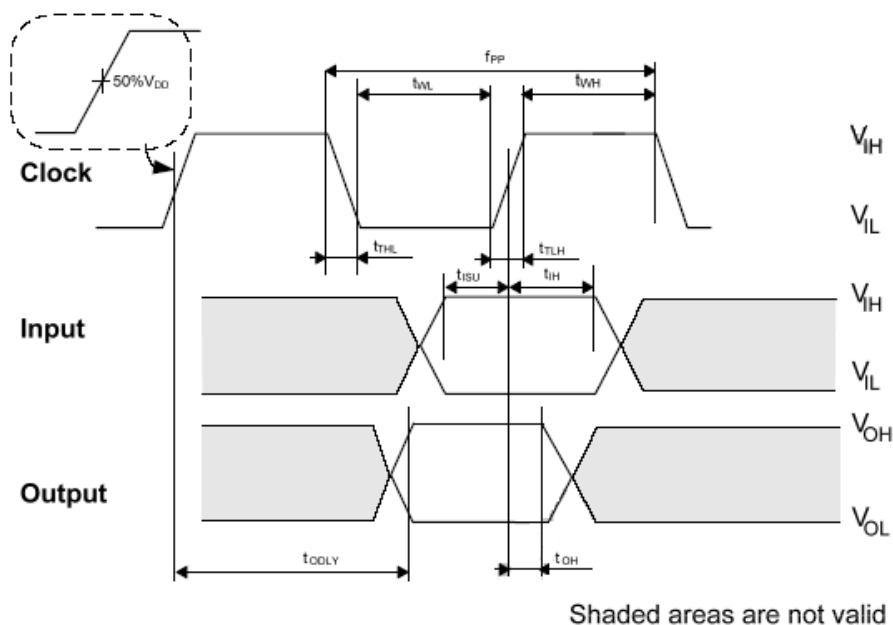
I1. Micro SD Interface timing (Default)



Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
Clock frequency Data Transfer Mode	f _{PP}	0	25	MHZ	C _{card} ≤ 10 pF (1 card)
Clock frequency Identification Mode	f _{OD}	0 ₍₁₎ /100	400	KHZ	C _{card} ≤ 10 pF (1 card)
Clock low time	t _{WL}	10		ns	C _{card} ≤ 10 pF (1 card)
Clock high time	t _{WH}	10		ns	C _{card} ≤ 10 pF (1 card)
Clock rise time	t _{TLH}		10	ns	C _{card} ≤ 10 pF (1 card)
Clock fall time	t _{THL}		10	ns	C _{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t _{ISU}	5		ns	C _{card} ≤ 10 pF (1 card)
Input hold time	t _{IH}	5		ns	C _{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t _{ODLY}	0	14	ns	C _L ≤ 40 pF (1 card)
Output Delay time during Identification Mode	t _{ODLY}	0	50	ns	C _L ≤ 40 pF (1 card)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

I2. Micro SD Interface timing (High-speed Mode)

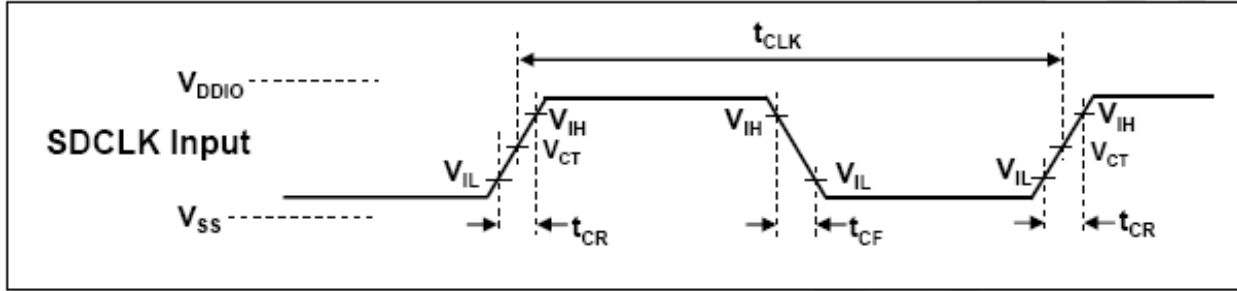


Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
Clock frequency Data Transfer Mode	f _{PP}	0	50	MHz	C _{card} ≤ 10 pF (1 card)
Clock low time	t _{WL}	7		ns	C _{card} ≤ 10 pF (1 card)
Clock high time	t _{WH}	7		ns	C _{card} ≤ 10 pF (1 card)
Clock rise time	t _{TLH}		3	ns	C _{card} ≤ 10 pF (1 card)
Clock fall time	t _{THL}		3	ns	C _{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t _{ISU}	6		ns	C _{card} ≤ 10 pF (1 card)
Input hold time	t _{IH}	2		ns	C _{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t _{ODLY}		14	ns	C _L ≤ 40 pF (1 card)
Output Hold time	T _{OH}	2.5		ns	C _L ≤ 15 pF (1 card)
Total System capacitance of each line ¹	C _L		40	pF	C _L ≤ 15 pF (1 card)

(1) In order to satisfy severe timing, host shall drive only one card.

I3. SD Interface timing (SDR12, SDR25, SDR50 and SDR104 Modes)

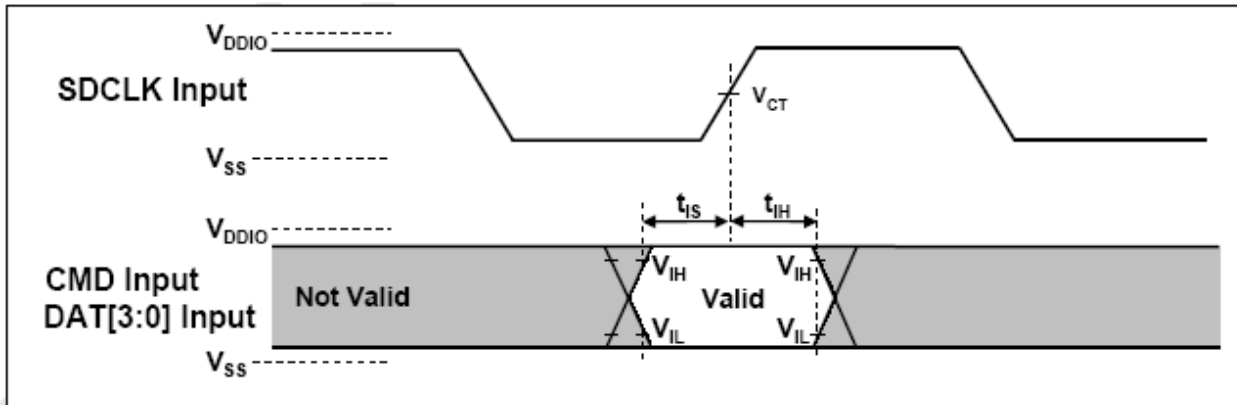
Input:



Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, $V_{CT}=0.975V$
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00ns$ (max.) at 100MHz, $CCARD=10pF$
Clock Duty	30	70	%	

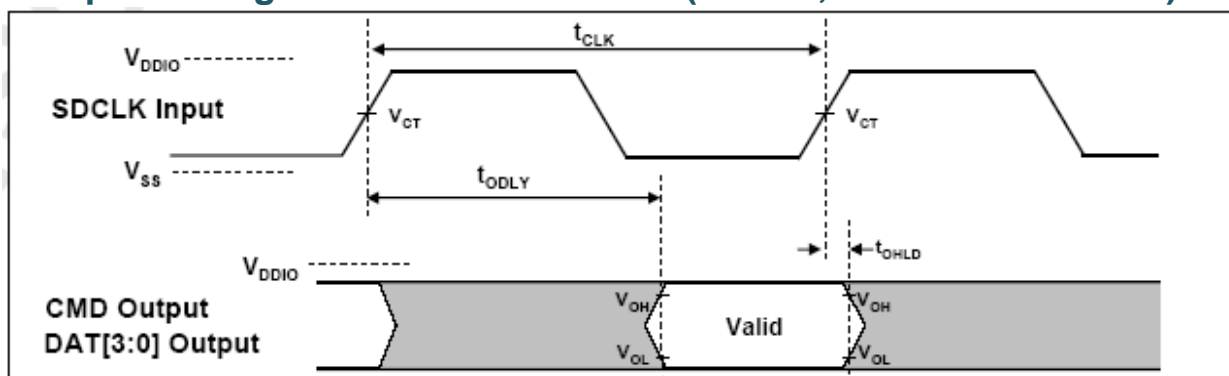
Clock Signal Timing

SDR50 and SDR104 Input Timing:



Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	$CCARD = 10pF, V_{CT} = 0.975V$
t_{IH}	0.80	-	ns	$CCARD = 5pF, V_{CT} = 0.975V$
Symbol	Min	Max	Unit	SDR50 Mode
t_{IS}	3.00	-	ns	$CCARD = 10pF, V_{CT} = 0.975V$
t_{IH}	0.80	-	ns	$CCARD = 5pF, V_{CT} = 0.975V$

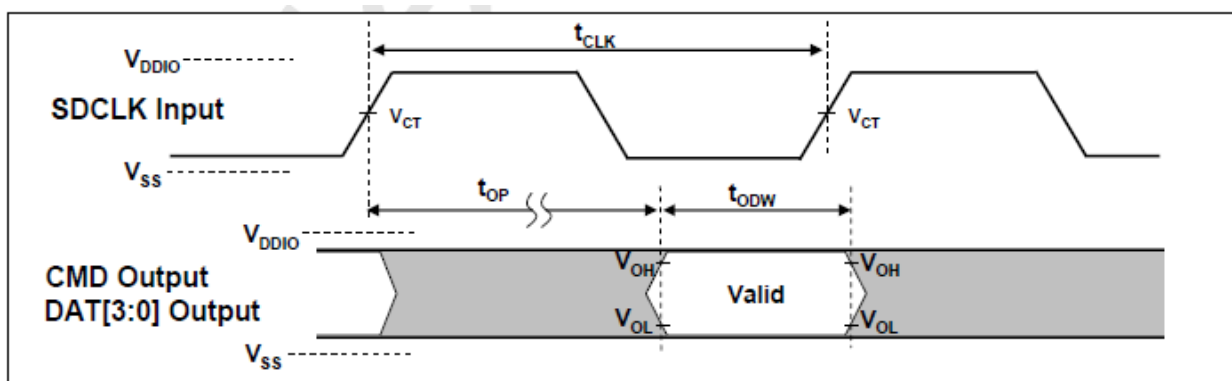
Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50):



Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	$t_{CLK} \geq 10.0\text{ns}$, $CL=30\text{pF}$, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	$t_{CLK} \geq 20.0\text{ns}$, $CL=40\text{pF}$, using driver Type B, for SDR25 and SDR12,
TOH	1.5	-	ns	Hold time at the t_{ODLY} (min.), $CL=15\text{pF}$

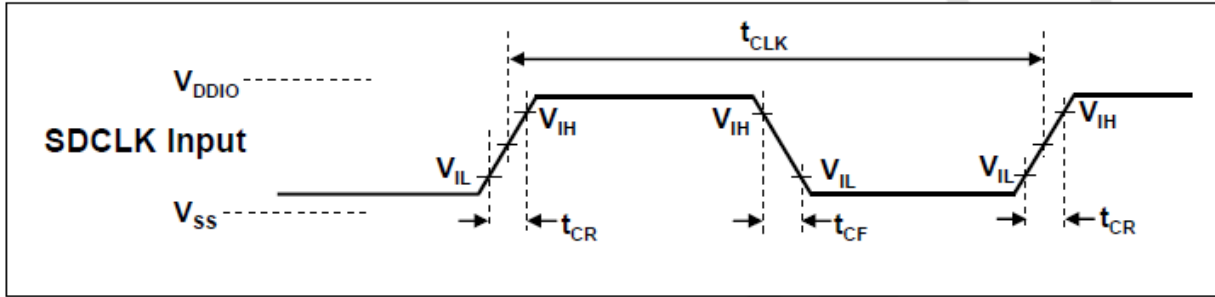
Output Timing of Fixed Data Window

Output Timing of Variable Window (SDR104):



Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	$t_{ODW}=2.88\text{ns}$ at 208MHz

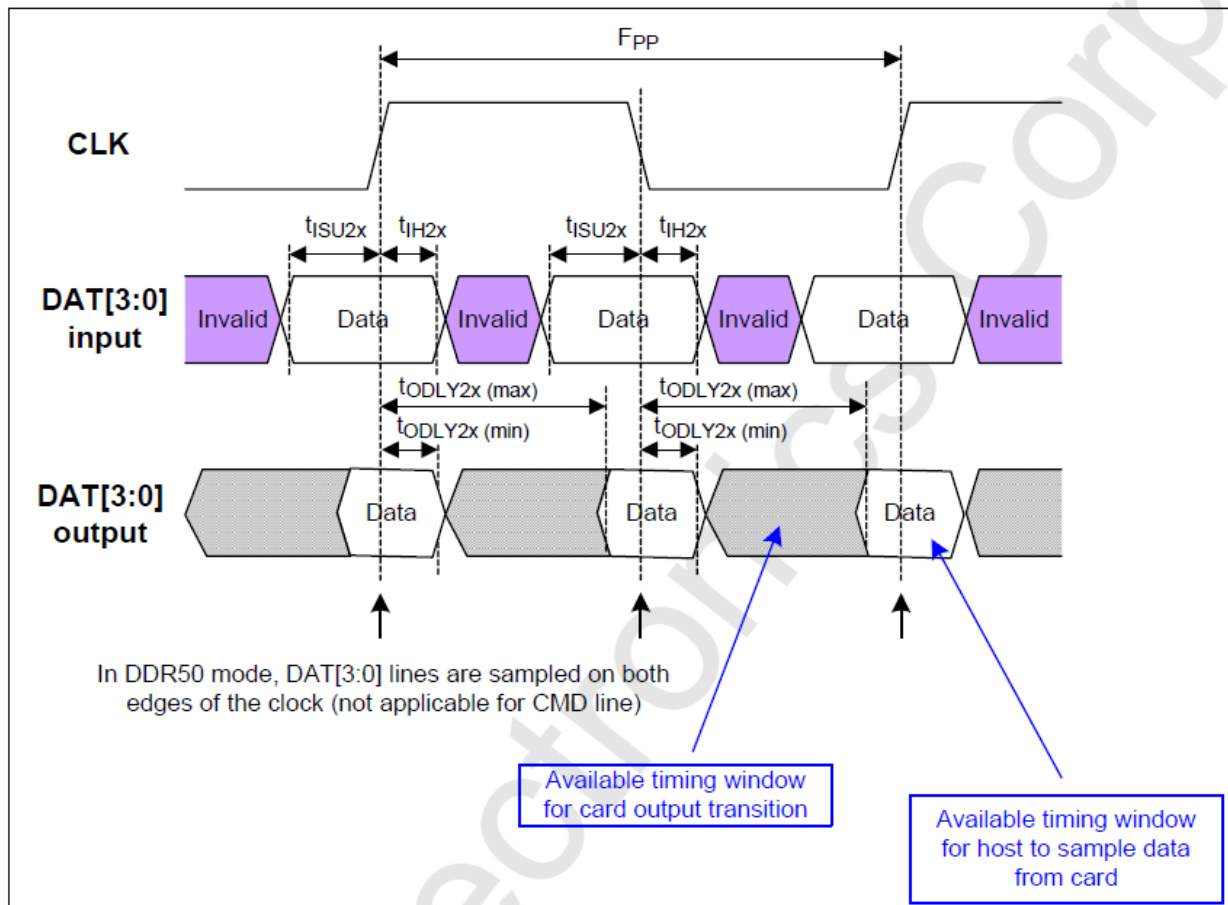
14. SD Interface timing (DDR50 Modes)



Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t _{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t _{CR} , t _{CF}	-	0.2 * t _{CLK}	ns	t _{CR} , t _{CF} < 4.00ns (max.) at 50MHz, CCARD=10pF
Clock Duty	45	55	%	

Clock Signal Timing

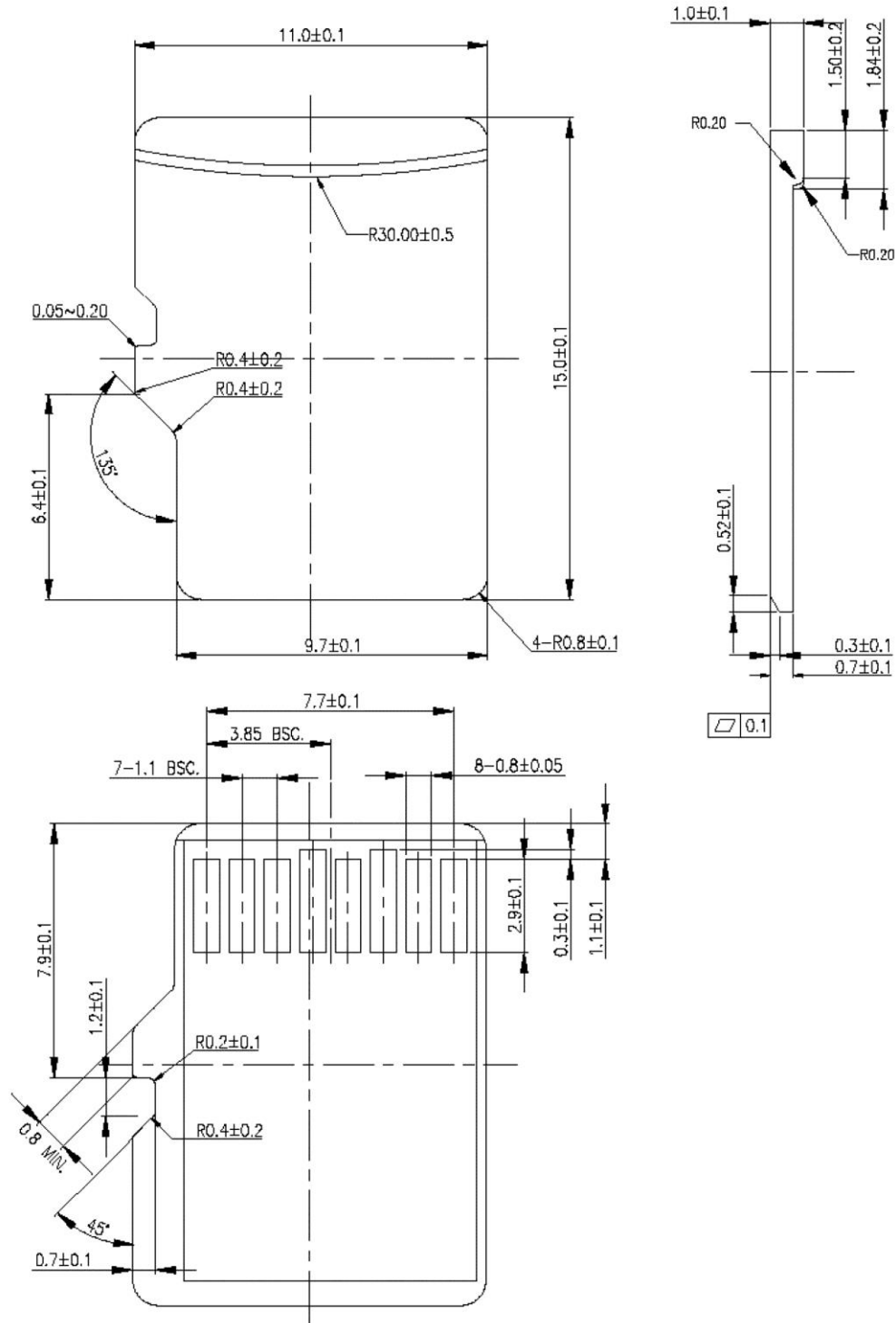


Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	6	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	$C_L \leq 30$ pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	$C_L \geq 15$ pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	$C_L \leq 25$ pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	$C_L \geq 15$ pF (1 card)

Bus Timings – Parameters Values (DDR50 mode)

J. Dimension



K Ordering information

PART NUMBER	DESCRIPTION
SLC – C TEMP μ SD CARDS	
EN-L0J128MDSC	128MB SLC μ SD CARD C TEMP
EN-L0J256MDSC	256MB SLC μ SD CARD C TEMP
EN-L0J512MDSC	512MB SLC μ SD CARD C TEMP
EN-L0J001GDSC	1GB SLC μ SD CARD C TEMP
EN-L0J002GDSC	2GB SLC μ SD CARD C TEMP
EN-L0J004GDSC	4GB SLC μ SD CARD C TEMP

PART NUMBER	DESCRIPTION
SLC – I TEMP μ SD CARDS	
EN-L0J128MDSI	128MB SLC μ SD CARD I TEMP
EN-L0J256MDSI	256MB SLC μ SD CARD I TEMP
EN-L0J512MDSI	512MB SLC μ SD CARD I TEMP
EN-L0J001GDSI	1GB SLC μ SD CARD I TEMP
EN-L0J002GDSI	2GB SLC μ SD CARD I TEMP
EN-L0J004GDSI	4GB SLC μ SD CARD I TEMP

PART NUMBER	DESCRIPTION
MLC – C TEMP μ SD CARDS	
EN-L0J002GDMC	2GB MLC μ SD CARD C TEMP
EN-L0J004GDMC	4GB MLC μ SD CARD C TEMP
EN-L0J008GDMC	8GB MLC μ SD CARD C TEMP
EN-L0J004GDMC	4GB MLC μ SD CARD C TEMP
EN-L0J008GDMC	8GB MLC μ SD CARD C TEMP
EN-L0J016GDMC	16GB MLC μ SD CARD C TEMP
EN-L0J032GDMC	32GB MLC μ SD CARD C TEMP
EN-L0J064GDMC	64GB MLC μ SD CARD C TEMP
EN-L0J128GDMC	128GB MLC μ SD CARD C TEMP
EN-L0J256GDMC	256GB MLC μ SD CARD C TEMP
EN-L0J512GDMC	512GB MLC μ SD CARD C TEMP

PART NUMBER	DESCRIPTION
MLC – I TEMP μ SD CARDS	
EN-L0J002GDMI	2GB MLC μ SD CARD I TEMP
EN-L0J004GDMI	4GB MLC μ SD CARD I TEMP
EN-L0J008GDMI	8GB MLC μ SD CARD I TEMP
EN-L0J004GDMI	4GB MLC μ SD CARD I TEMP
EN-L0J008GDMI	8GB MLC μ SD CARD I TEMP
EN-L0J016GDMI	16GB MLC μ SD CARD I TEMP
EN-L0J032GDMI	32GB MLC μ SD CARD I TEMP

PART NUMBER	DESCRIPTION
TLC – C TEMP μSD CARDS	
EN-L0J002GDTC	2GB TLC μSD CARD C TEMP
EN-L0J004GDTC	4GB TLC μSD CARD C TEMP
EN-L0J008GDTC	8GB TLC μSD CARD C TEMP
EN-L0J004GDTC	4GB TLC μSD CARD C TEMP
EN-L0J008GDTC	8GB TLC μSD CARD C TEMP
EN-L0J016GDTC	16GB TLC μSD CARD C TEMP
EN-L0J032GDTC	32GB TLC μSD CARD C TEMP
EN-L0J064GDTC	64GB TLC μSD CARD C TEMP
EN-L0J128GDTC	128GB TLC μSD CARD C TEMP
EN-L0J256GDTC	256GB TLC μSD CARD C TEMP
EN-L0J512GDTC	512GB TLC μSD CARD C TEMP
EN-L0J001TDTC	1TB TLC μSD CARD C TEMP